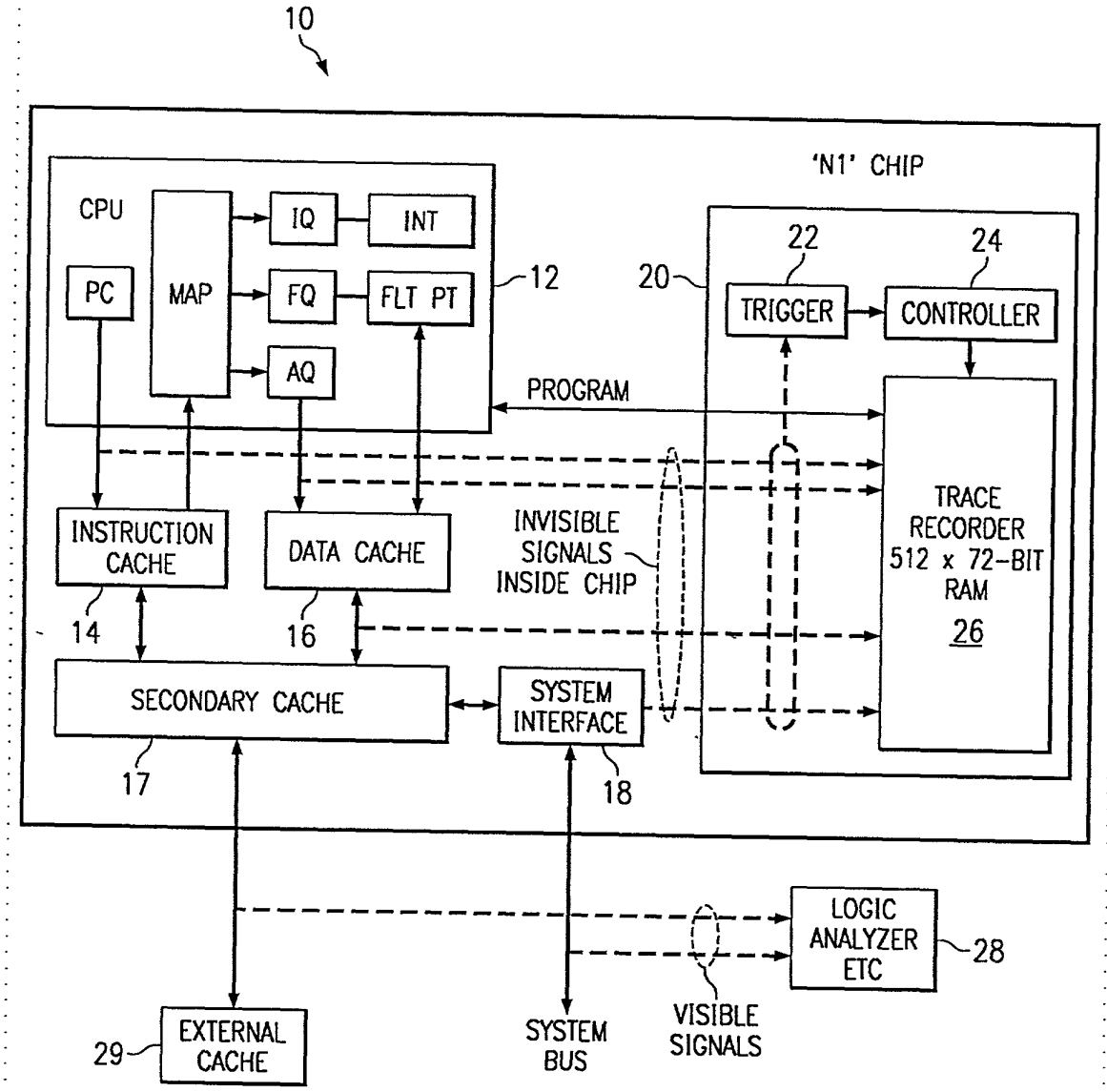

10
'N1' CHIP
CPU
PC
MAP
IQ
INT
FQ
FLT PT
AQ
12
20
22
24
TRIGGER
CONTROLLER
PROGRAM
TRACE
RECORDER
512 x 72-BIT
RAM
26
INSTRUCTION
CACHE
DATA CACHE
INVISIBLE
SIGNALS
INSIDE CHIP
14
16
SECONDARY CACHE
SYSTEM
INTERFACE
17
18
LOGIC
ANALYZER
ETC
28
29
EXTERNAL
CACHE
SYSTEM
BUS
VISIBLE
SIGNALS

FIG. 1

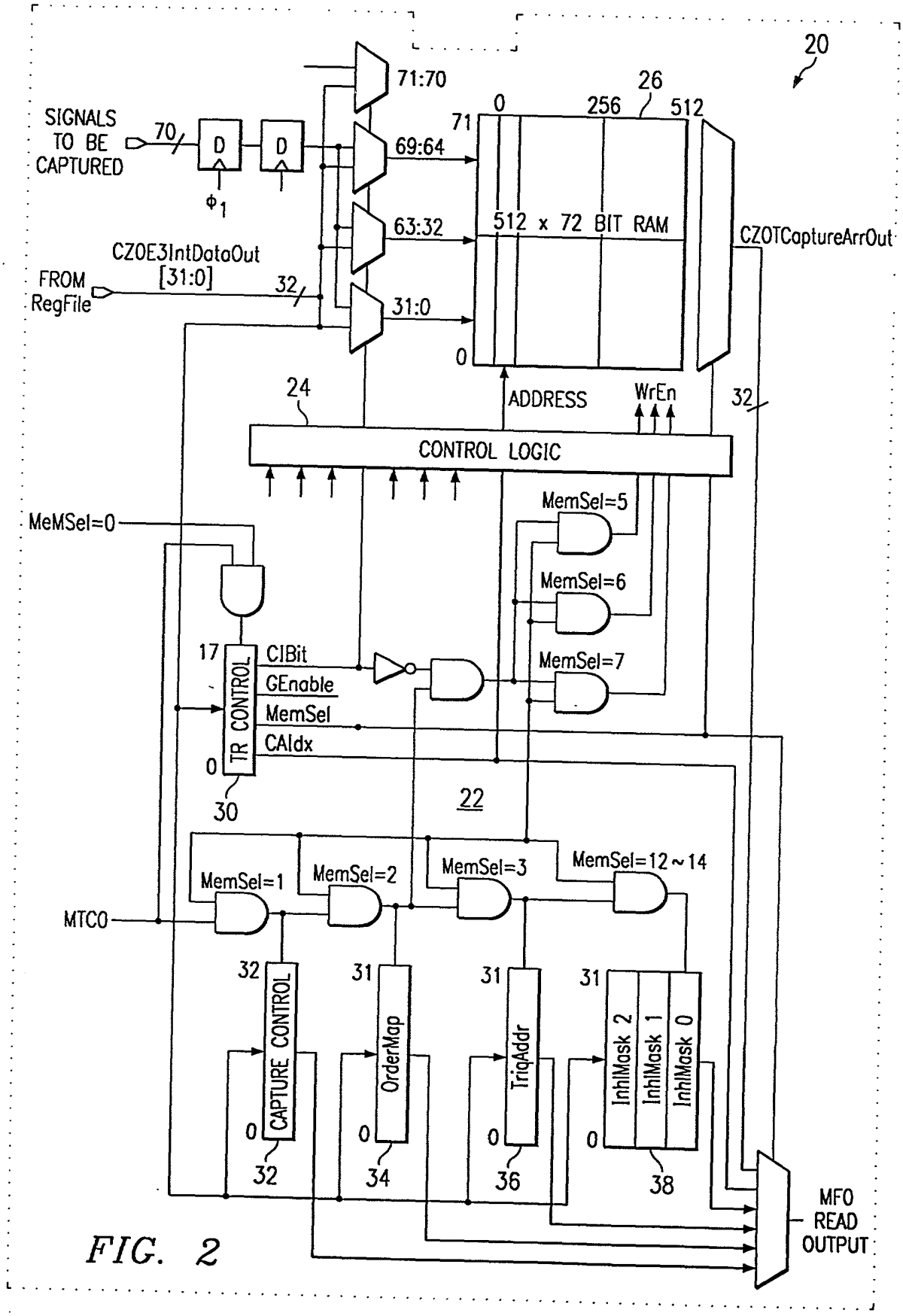

20
SIGNALS TO BE CAPTURED
70
D
D
Φ_1
71:70
69:64
63:32
31:0
26
0
256
512
71
512 x 72 BIT RAM
CZOTCaptureArrOut
CZOE3IntDataOut [31:0]
FROM RegFile
32
0
24
ADDRESS
WrEn
32
CONTROL LOGIC
MeMSel=0
MemSel=5
MemSel=6
MemSel=7
17
TR CONTROL
CIBit
GEnable
MemSel
CAIdx
0
30
22
MemSel=1
MemSel=2
MemSel=3
MemSel=12~14
MTCO
32
CAPTURE CONTROL
31
OrderMap
31
TriqAddr
31
InhlMask 2
InhlMask 1
InhlMask 0
0
32
34
36
38
MFO READ OUTPUT

FIG. 2

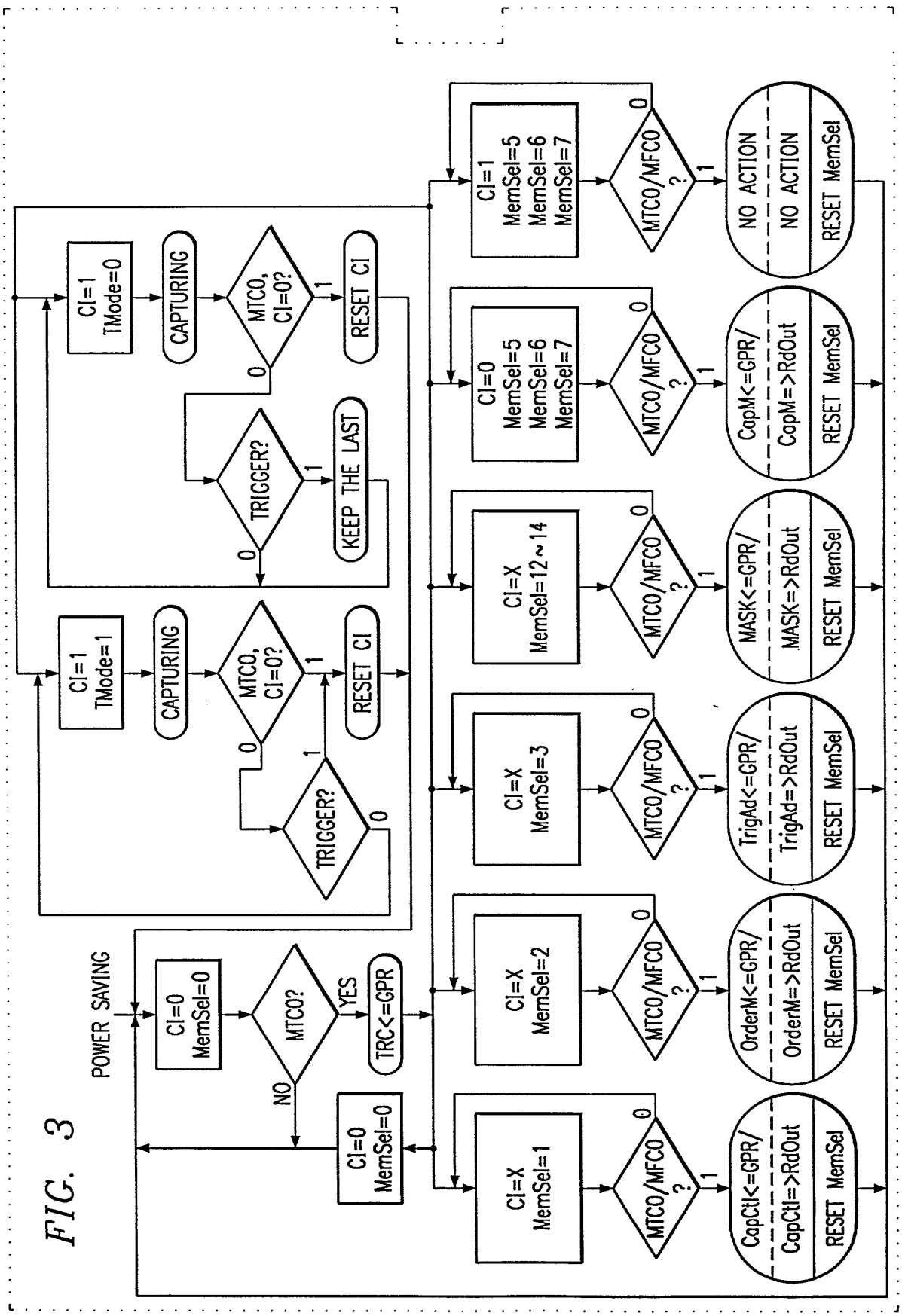

POWER SAVING
CI=0
MemSel=0
MTC0?
YES
NO
TRC<=GPR
CI=0
MemSel=0
CI=1
TMode=1
CAPTURING
MTC0,
CI=0?
TRIGGER?
RESET CI
CI=1
TMode=0
CAPTURING
MTC0,
CI=0?
TRIGGER?
KEEP THE LAST
RESET CI
CI=X
MemSel=1
MTC0/MFC0
?
CapCtl<=GPR/
CapCtl=>RdOut
RESET MemSel
CI=X
MemSel=2
MTC0/MFC0
?
OrderM<=GPR/
OrderM=>RdOut
RESET MemSel
CI=X
MemSel=3
MTC0/MFC0
?
TrigAd<=GPR/
TrigAd=>RdOut
RESET MemSel
CI=X
MemSel=12~14
MTC0/MFC0
?
MASK<=GPR/
MASK=>RdOut
RESET MemSel
CI=0
MemSel=5
MemSel=6
MemSel=7
MTC0/MFC0
?
CapM<=GPR/
CapM=>RdOut
RESET MemSel
CI=1
MemSel=5
MemSel=6
MemSel=7
MTC0/MFC0
?
NO ACTION
NO ACTION
RESET MemSel

FIG. 3

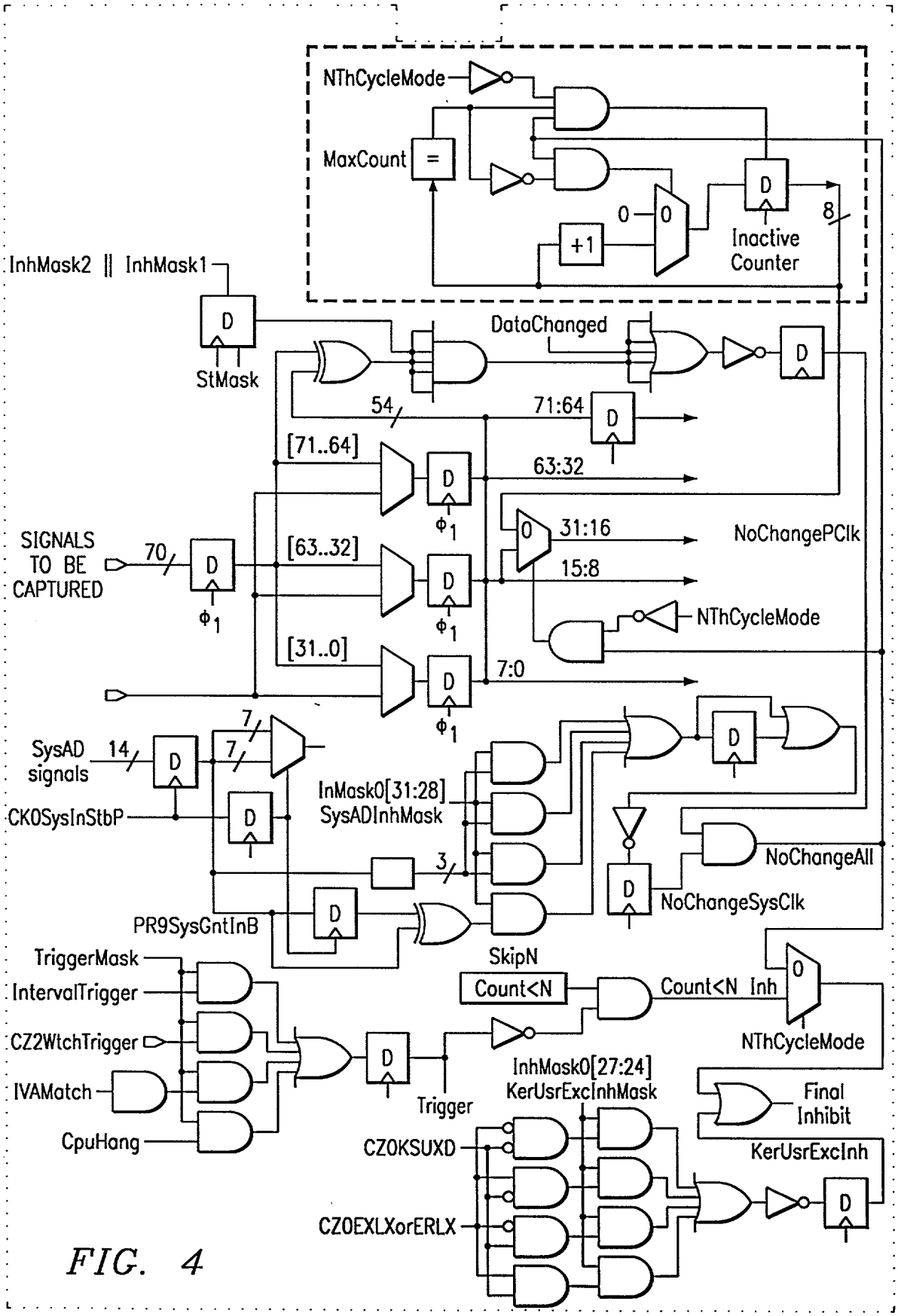

NThCycleMode
MaxCount
=
+1
0
0
D
8
Inactive Counter
InhMask2 || InhMask1
D
StMask
DataChanged
D
54
71:64
D
[71..64]
63:32
D
ϕ_1
0
31:16
NoChangePClk
SIGNALS TO BE CAPTURED
70
D
ϕ_1
[63..32]
D
ϕ_1
15:8
NThCycleMode
[31..0]
D
ϕ_1
7:0
7
SysAD signals
14
D
7
CK0SysInStbP
D
InMask0[31:28]
SysADInhMask
D
3
NoChangeAll
D
NoChangeSysClk
PR9SysGntInB
D
SkipN
TriggerMask
IntervalTrigger
CZ2WtchTrigger
IVAMatch
CpuHang
Count<N
Count<N Inh
0
NThCycleMode
D
Trigger
InhMask0[27:24]
KerUsrExcInhMask
Final Inhibit
CZ0KSUXD
KerUsrExcInh
CZ0EXLXorERLX
D

FIG. 4

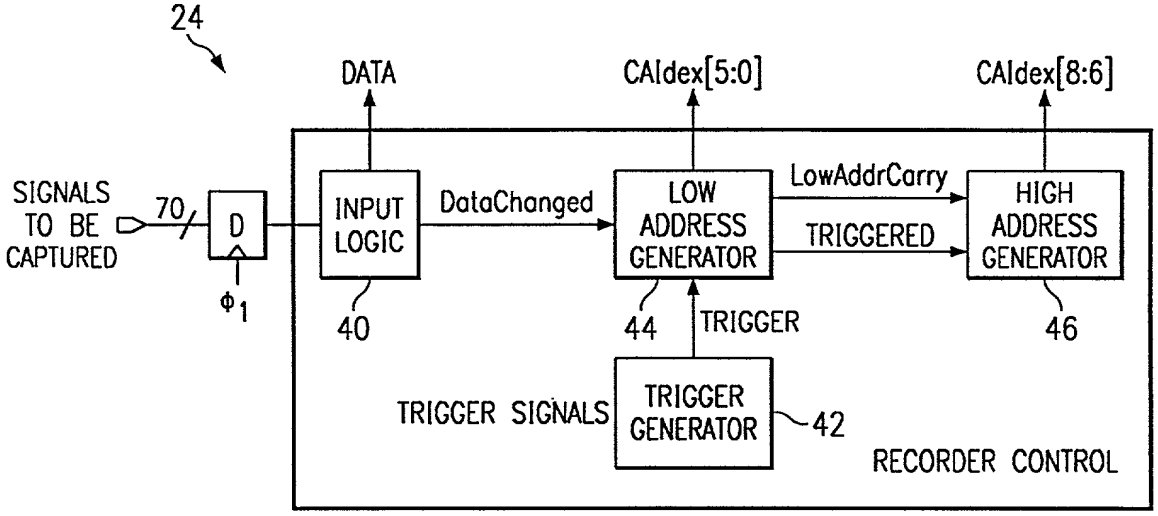

24
DATA
CAIdex[5:0]
CAIdex[8:6]
SIGNALS TO BE CAPTURED
70
D
Φ_1
INPUT LOGIC
40
DataChanged
LOW ADDRESS GENERATOR
44
LowAddrCarry
TRIGGERED
HIGH ADDRESS GENERATOR
46
TRIGGER
TRIGGER SIGNALS
TRIGGER GENERATOR
42
RECORDER CONTROL

FIG. 5

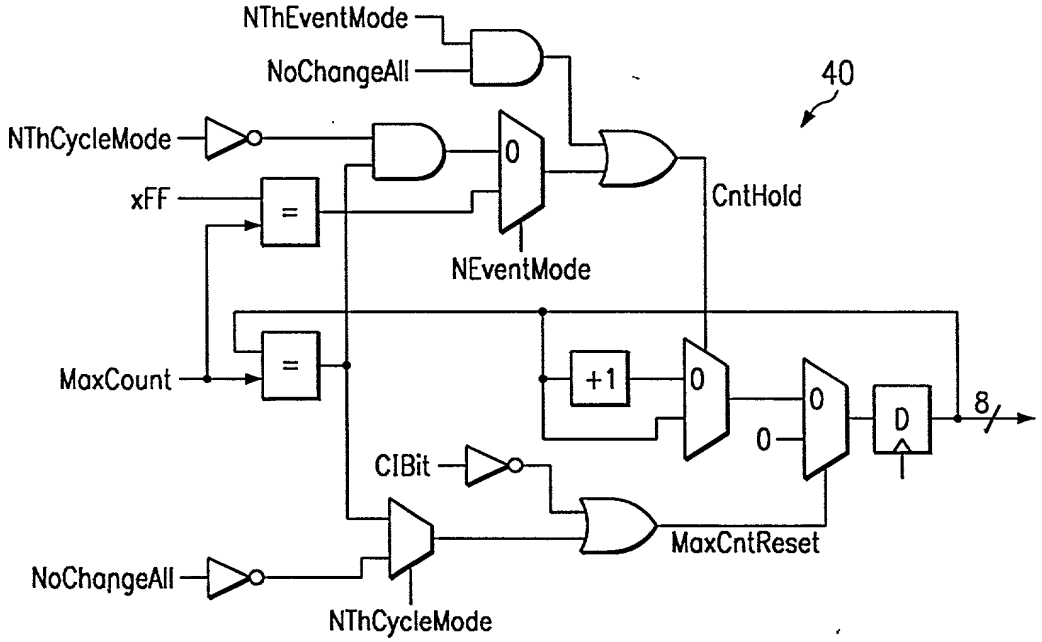

NThEventMode
NoChangeAll
40
NThCycleMode
xFF
=
0
CntHold
NEventMode
MaxCount
=
+1
0
0
0
D
8
CIBit
MaxCntReset
NoChangeAll
NThCycleMode

FIG. 6

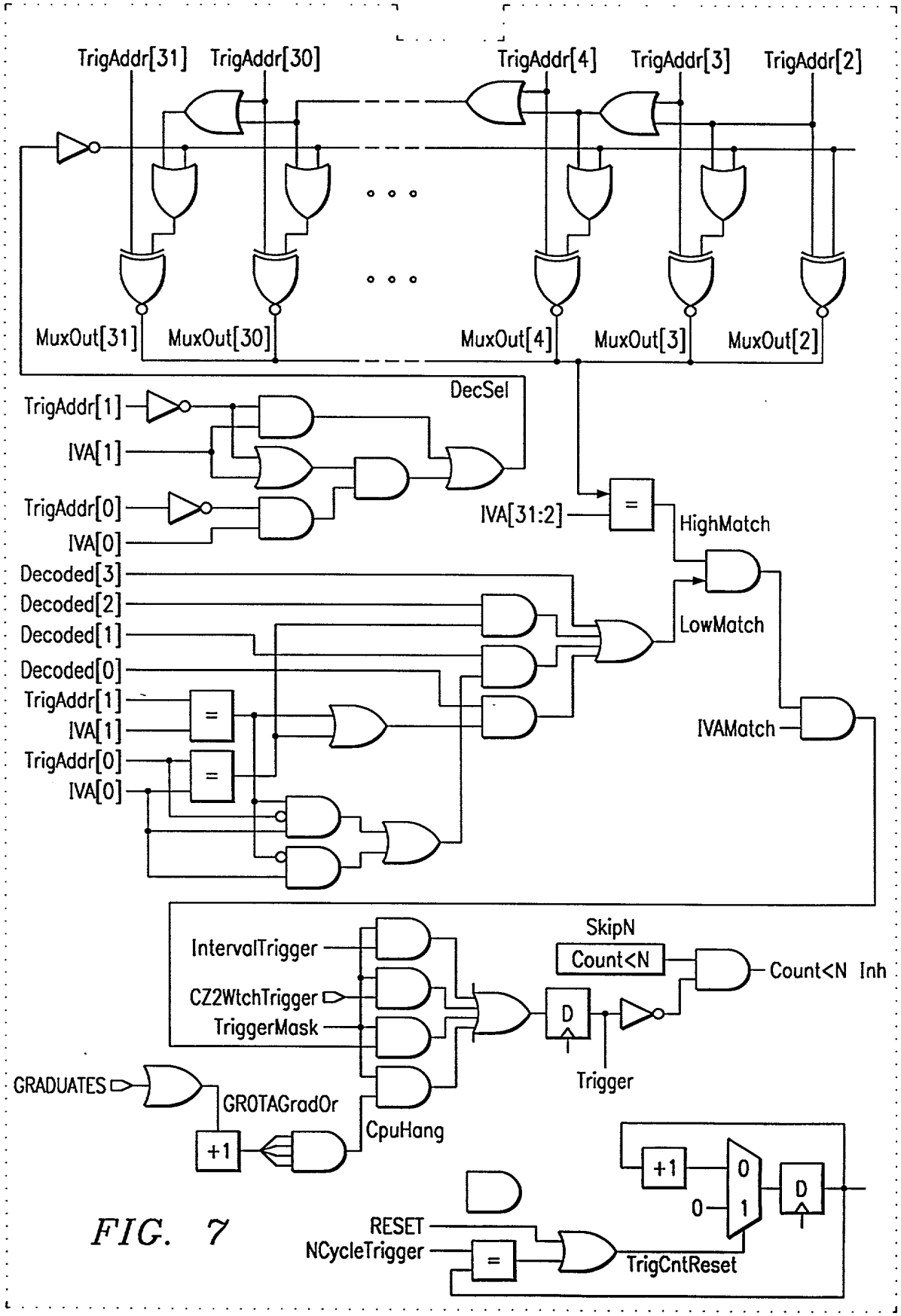

TrigAddr[31]
TrigAddr[30]
TrigAddr[4]
TrigAddr[3]
TrigAddr[2]
MuxOut[31]
MuxOut[30]
MuxOut[4]
MuxOut[3]
MuxOut[2]
DecSel
TrigAddr[1]
IVA[1]
TrigAddr[0]
IVA[0]
IVA[31:2]
=
HighMatch
Decoded[3]
Decoded[2]
Decoded[1]
Decoded[0]
LowMatch
TrigAddr[1]
IVA[1]
TrigAddr[0]
IVA[0]
=
=
IVAMatch
SkipN
IntervalTrigger
Count<N
Count<N Inh
CZ2WtchTrigger
TriggerMask
D
Trigger
GRADUATES
GROTAGradOr
CpuHang
+1
+1
0
1
D
RESET
NCycleTrigger
=
TrigCntReset

FIG. 7

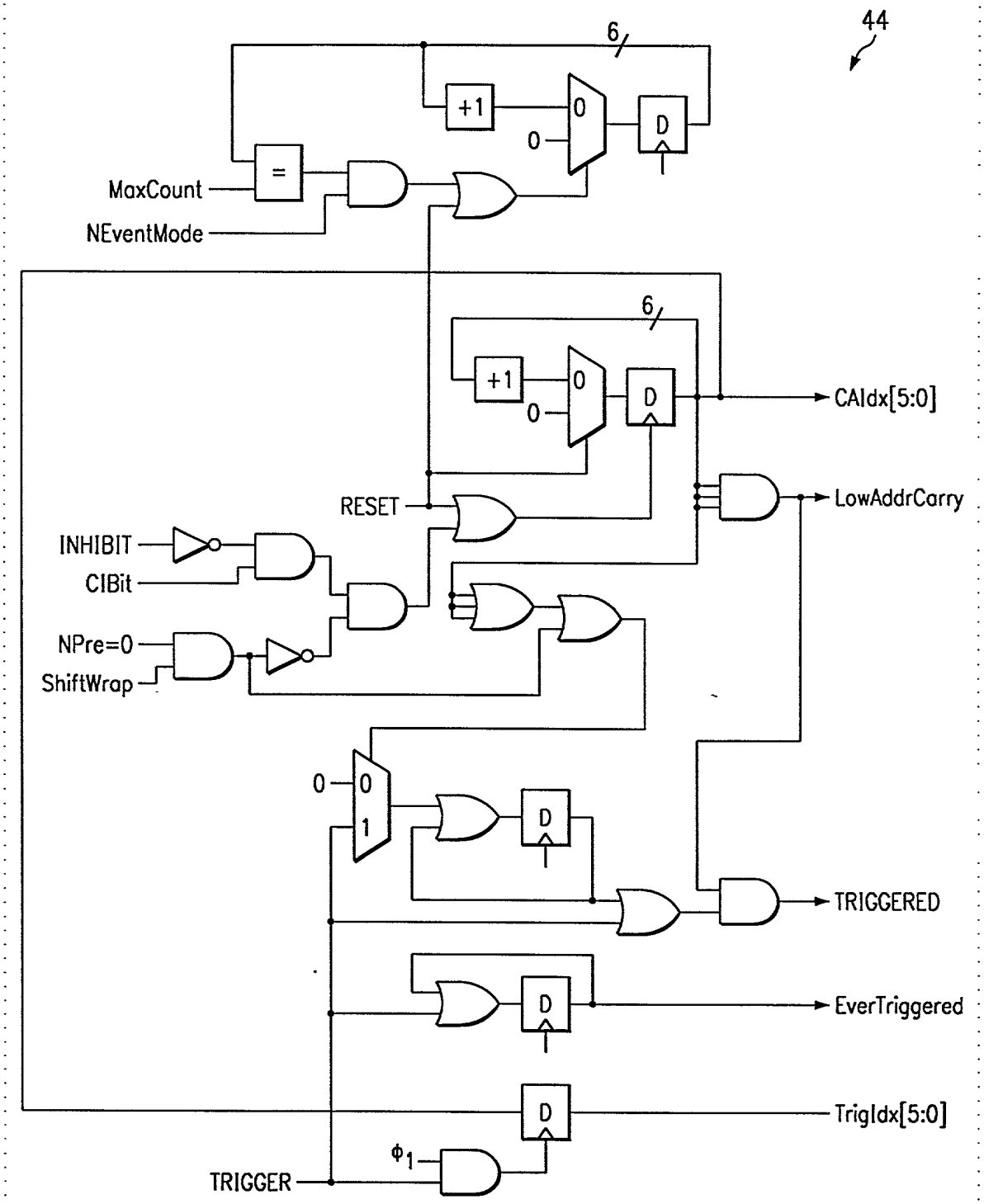
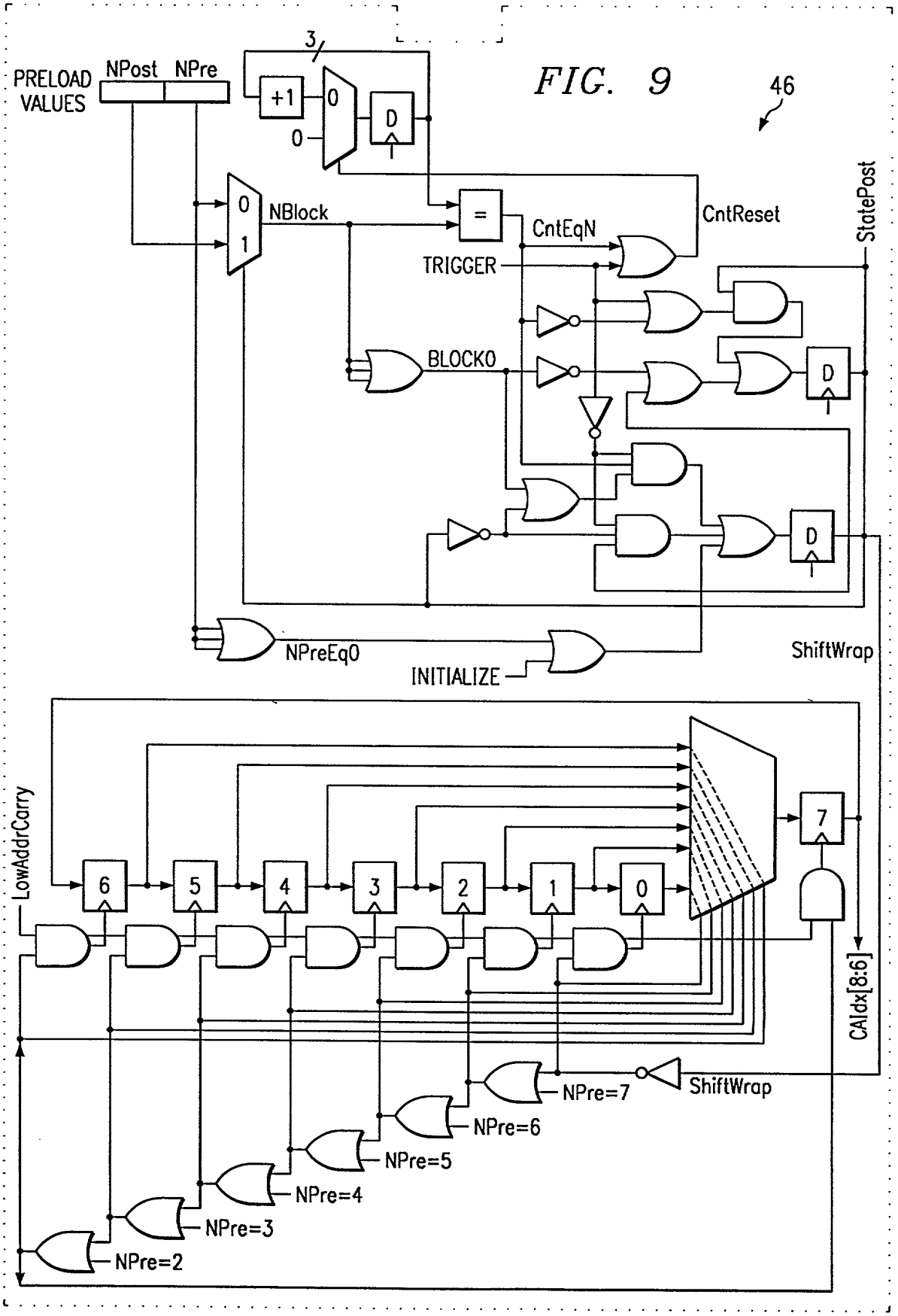

44
6
+1
0
0
D
=
MaxCount
NEventMode
6
+1
0
0
D
CAIdx[5:0]
RESET
LowAddrCarry
INHIBIT
CIBit
NPre=0
ShiftWrap
0
0
1
D
TRIGGERED
D
EverTriggered
D
TrigIdx[5:0]
ϕ_1
TRIGGER

FIG. 8

FIG. 9


PRELOAD VALUES
NPost
NPre
3
+1
0
D
0
1
NBlock
=
CntEqN
CntReset
StatePost
TRIGGER
BLOCK0
D
D
NPreEq0
INITIALIZE
ShiftWrap
LowAddrCarry
6
5
4
3
2
1
0
7
CAIdx[8:6]
NPre=7
ShiftWrap
NPre=6
NPre=5
NPre=4
NPre=3
NPre=2

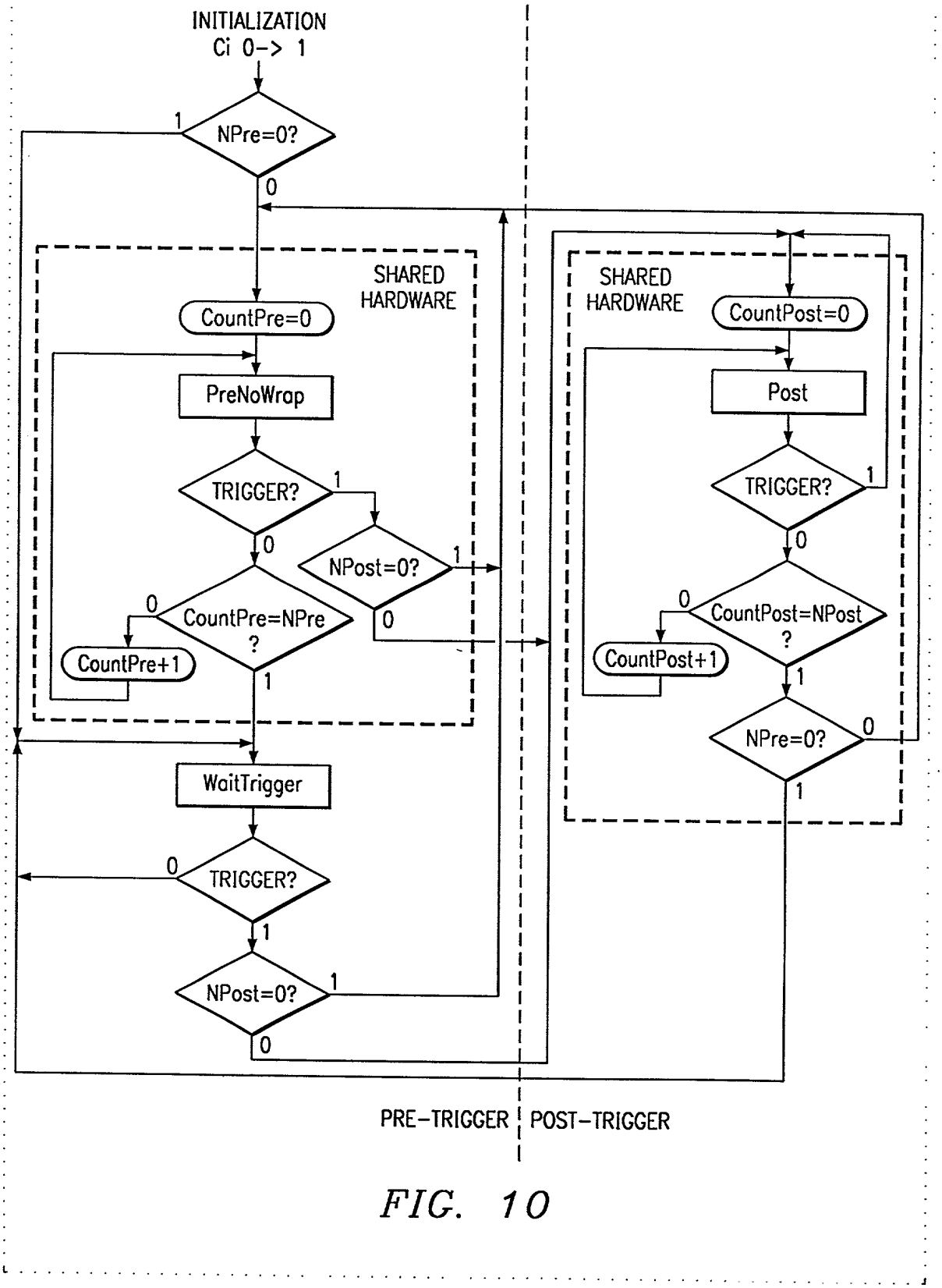

INITIALIZATION
Ci 0-> 1
NPre=0?
SHARED HARDWARE
CountPre=0
PreNoWrap
TRIGGER?
NPost=0?
CountPre=NPre ?
CountPre+1
WaitTrigger
TRIGGER?
NPost=0?
SHARED HARDWARE
CountPost=0
Post
TRIGGER?
CountPost=NPost ?
CountPost+1
NPre=0?
PRE-TRIGGER
POST-TRIGGER

FIG. 10